In the Claims:

Please amend the claims as indicated below.

1. (currently amended) A transistor memory array comprising:

a first plurality of non-volatile user programmable memory ~~transistors~~ cells including a memory transistor and a select transistor and a second plurality of mask programmed read-only memory ~~transistors~~ cells including a memory transistor and a select transistor, the non-volatile memory ~~transistors~~ cells and the read-only memory ~~transistors~~ cells having the same footprint within a single memory array.

2. (cancelled)

3. (currently amended) The memory array of claim [[2]] 1 wherein said footprint has a longitudinal dimension and a width dimension that are the same for both the first and second pluralities of memory cells ~~transistors~~, with the select transistor and memory transistor having a common electrode in each memory cell.

4. (currently amended) The memory array of claim 1 wherein the read-only memory cells ~~transistors~~ include cells having transistors with substrates having open channels and cells having transistors with substrates having shorted channels.

5. (currently amended) The memory array of claim 1 wherein the non-volatile memory ~~transistors~~ cells have two poly layers and the read-only memory ~~transistors~~ cells have one poly layer.

6. (currently amended) The memory array of claim 1 wherein the second plurality of read-only memory ~~transistors~~ cells is grouped into rows.

7. (currently amended) The memory array of claim 6 wherein said group of rows of read only ~~transistors~~ memory cells has a first subgroup of transistors in at least one row in a first logic state.

8. (currently amended) The memory array of claim 7 wherein said group of rows of read-only memory ~~transistors~~ cells has a second subgroup of transistors in at least one row in a second logic state.

9. (currently amended) The memory array of claim 4 wherein the channels in the transistors in the read-only memory ~~transistors~~ cells are defined by a buried depletion implant in said substrate, the extent of the implant defining open and shorted channels.

10. (currently amended) The transistor array of claim 1 wherein said non-volatile memory ~~transistors are~~ cells have EEPROM transistors.

11. (withdrawn) A method of making a transistor memory array with both read-only memory and rewriteable MOS and CMOS memory transistors, all having subsurface electrodes and channels comprising:

providing a single mask set for forming a memory array of rows and columns of memory transistor sites, at least including masks for forming a subsurface active region, heavily doped first and second, spaced apart depletion implant subsurface regions in the active region defining a channel therebetween, a thin oxide layer, a first polysilicon layer and a second polysilicon layer spaced apart from and over the first polysilicon layer;

for a first set of memory transistor sites, blocking mask portions for forming the second depletion implant subsurface region to the extent that the channel is extended

to impede transistor conductivity, the mask set further modified by blocking formation of the thin oxide layer and the first polysilicon layer, thereby forming read-only memory transistor cells that are open at the first set of sites;

for a second set of memory transistor sites, increasing the first and second depletion implant subsurface regions to the extent that the channel is shorted to establish permanent transistor conductivity at the second set of sites, the mask set further modified by blocking formation of the thin oxide layer and the first polysilicon layer; and

for a third set of memory transistor sites, using the single mask set to form EEPROM memory transistor cells.

12. (withdrawn) The method of claim 11 further defined by grouping the first and second sets of memory transistor sites in a first group of rows and grouping the EEPROM memory transistors in a second group of rows.

13. (withdrawn) The method of claim 11 further defined by establishing an active region using the single mask set and forming a select transistor adjacent to the memory transistor.

14. (withdrawn) The method of claim 13 further defined by forming the active region as a longitudinal region with opposed edges, the active region having buried n subsurface regions for at least the memory transistors.

15. (withdrawn) A method of making a transistor memory array comprising:

establishing an array with rows and columns of memory cells, each cell having an active area of a specified longitudinal dimension sufficient in length for formation of both a non-volatile memory cell and a read- only memory cell.

16. (withdrawn) The method of claim 15 wherein the memory array comprises rows and columns of transistor cells with a first plurality of rows of non-volatile memory cells and a second plurality of read-only memory transistor cells.

17. (withdrawn) The method of claim 15 further defined by forming a select transistor within the active area for both non-volatile memory transistor cells and read-only memory transistor cells.

18. (withdrawn) The method of claim 15 further defined by providing two poly layers for the plurality of non-volatile memory transistor cells and a single poly layer for the read-only memory transistor cells.

19. (withdrawn) The method of claim 16 further defined by programming the read-only memory transistor cells at the time of manufacture with pre-defined data consisting of ones and zeros.

20. (previously presented) A transistor memory array comprising:

a plurality of memory cells all having the same areawise footprint including first memory cells having a user programmable EEPROM transistor, second memory cells having a mask programmed read only memory transistor in a first logic state, and third memory cells having a mask programmed read only memory transistor in a second logic state.

21. (previously presented) The transistor memory array of claim 20 wherein each memory cell has a select transistor communicating with the memory transistor.

22. (previously presented) The transistor memory array of claim 20 wherein said read only memory transistors are in a row.

23. (previously presented) The transistor memory array of claim 20 wherein the memory cells having a read only memory transistor in a first logic state have a permanently open channel.

24. (previously presented) The transistor memory array of claim 20 wherein the memory cells having a read only memory transistor in a second logic state have a permanently shorted channel.

25. (previously presented) A transistor memory array comprising diverse memory cells in a memory array all having the same areawise footprint, a first group of memory cells being user programmable and a second group of memory cells being mask programmed.

26. (previously presented) The memory cell of claim 25 wherein said diverse memory cells comprise non-volatile memory transistors and read only memory transistors.

27. (previously presented) The memory array of claim 26 wherein said read only memory transistors comprise a first group of transistors in a first logic state and a second group of transistors in a second logic state.

28. (previously presented) The memory array of claim 27 wherein each of the memory transistors in said first group is in a first common row and each of the memory transistors in the second group is in a second common row.

29. (previously presented) The memory array of claim 25 wherein each memory cell comprises a memory cell and a select transistor.

30. (previously presented) The memory array of claim 27 wherein the first group of memory transistors has open channels and the second group of memory transistors has shorted channels.